

## **REMARKS/ARGUMENTS**

Claims 1-20 were pending. Claims 1, 7 and 13 have been amended; claims 18-20 have been canceled without prejudice, and claims 21-23 have been added. Hence, claims 1-17 and 21-23 remain pending.

The Office Action of October 23, 2006 rejects claims 1-12 under 35 USC 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 6,549,049) in view of Cheung U.S. Patent No. 6,564,329). Claims 13-20 were rejected under 35 USC 103(a) as being unpatentable over Chang et al. (U.S. Patent Publication No. 2003/0135836) in view of Nadeau (US Patent Publication No. 2003/0146777). Applicant respectfully amends in part and traverses in part in addressing the rejections.

As amended, claim 1 provides delay equalizer for balancing clock signals in a clock tree that includes, *inter alia*, a multiplexer operable to receive a select control signal indicating which of a first output clock signal or a second output clock signal to select. The select control signal is programmable on the fly, and transitions only when the first output clock signal and the second output clock signal have the same phase. An example of such on the fly programmability is disclosed in Fig. 5 of the specification. None of the cited art discloses, teaches or suggests such controlled transition of the select control signal. Hence, Applicant respectfully requests withdrawal of the rejection of claim 1 and allowance thereof for at least this reason. Further, as claims 2-6 and 21-22 properly depend from an allowable base claim, Applicant respectfully requests withdrawal of the outstanding rejection and allowance thereof for at least this reason.

Further, claim 21 provides for transitioning the select control signal substantially coincident with a rising edge of the first output clock signal and a rising edge of the second output clock signal in the same phase. Cheung expressly teaches away from such an approach as it "may produce an undesirable glitch on the output". Cheung at col. 9, ll. 39-45. Instead, Cheung requires a delay introduced by switching on the falling edge of the master clock. Id. Hence, for at least this additional reason, Applicant respectfully asserts that claim 21 is in condition for allowance for at least this additional reason.

As amended, claim 7 provides a method for balancing clock signals in a node of a clock tree. The method includes, *inter alia*, receiving at a multiplexer a select control

signal indicating which of a first output clock signal or a second output clock signal to select. The select control signal is programmable on the fly, and transitions only when the first output clock signal and the second output clock signal have the same phase. None of the cited art discloses, teaches or suggests such on the fly programmability. Hence, Applicant respectfully requests withdrawal of the rejection of claim 7 and allowance thereof for at least this reason. Further, as claims 8-12 properly depend from an allowable base claim, Applicant respectfully requests withdrawal of the outstanding rejection and allowance thereof for at least this reason.

As amended, claim 13 provides a method for balancing one or more clock signals in a clock tree having a multi-mode clock distribution. The method includes, *inter alia*, associating a delay equalizer with each of one or more clock-dividing and selection modules in a clock tree. The delay equalizer is operable to substantially balance the one or more clock signals between two or more functional modes. The method further includes identifying a clock balance path that is selected based on a requirement of a particular one of the two or more functional modes; and determining one or more clock paths to be balanced with the clock balance path. Each of the one or more clock paths to be balanced includes a multi-mode dependant clock path, wherein the multi-mode dependant clock path includes the two or more functional modes. None of the cited art discloses, teaches or suggests the aforementioned process including the identification of a clock balance path. Hence, for at least this reason, Applicant respectfully requests withdrawal of the rejection of claim 13 and allowance thereof. Further, as claims 14-17 and 23 properly depend from an allowable base claim, Applicant respectfully requests withdrawal of the outstanding rejection and allowance thereof for at least this reason.

Further, claims 16-17 are improperly rejected. In particular, the Office Action points out that Nadeau “teaches the method comprising one or more exclusive-NOR (XNOR) gates (98, 100, 102) inserted throughout the clock tree”. Such a statement is not supportable. Rather, the aforementioned gates are respectively an AND gate, and OR gate, and another AND gate. As is well known, the aforementioned gates are not the same as an XNOR gate. Indeed, the explicit use of such gates would discourage the use of an XNOR gate. There is no motivation or suggestion to choose the specific operation of an XNOR gate based on the disclosure of Nadeau. Hence, for at least this additional

reason, Applicant respectfully requests withdrawal of the rejections of claims 16-17 and allowance thereof.

Also, the Office Action of October 23, 2006 is prematurely final adding art in such a way that precluded applicant's opportunity to respond. "While the rules no longer give to an applicant the right to 'amend as often as the examiner presents new references or reasons for rejection,' present practice does not sanction hasty and ill-considered final rejections. The applicant who is seeking to define his or her invention in claims that will give him or her the patent protection to which he or she is justly entitled should receive the cooperation of the examiner to that end, and not be prematurely cut off in the prosecution of his or her application." MPEP at 706.07. Accordingly, Applicant respectfully requests that the finality of the rejection be withdrawn.

## CONCLUSION

In view of the foregoing, Applicant respectfully asserts that all claims now pending in the application are in condition for allowance. Hence, an early allowance of all such claims is earnestly requested.

Applicant files a Request for Continued Examination (RCE) herewith, and to the extent necessary petitions for an extension of time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees under 37 CFR 1.136 and RCE fees, to the deposit account of the assignee, Texas Instruments Incorporated, Account No. 20-0668.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 720-266-4728.

Respectfully submitted,

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